

PHY latency and its effects on TSN performance

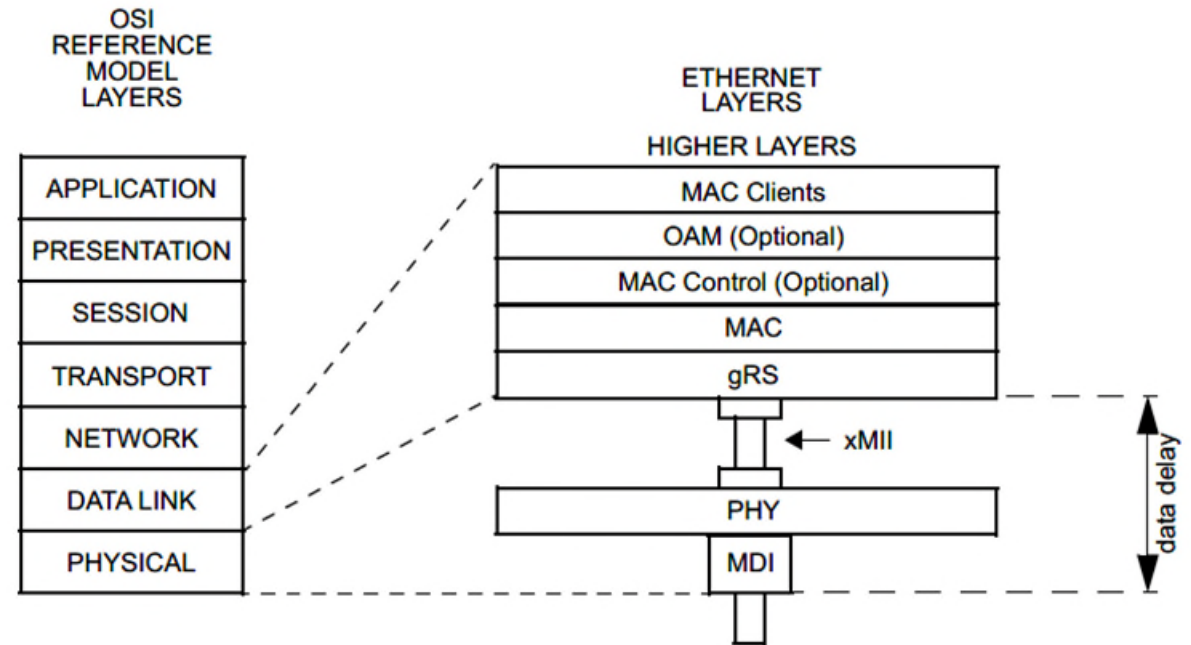
Alon Regev and Marty Gubow
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Agenda

- Delay measurement points
- How does PHY latency affect TSN performance
 - Effects on 802.1AS
 - Effects on 802.1Q scheduled traffic (802.1Qbv)
- 802.3cx and timestamping improvements
- PHY delay characterization
- Sample measurements
- Summary and recommendations

Delay Measurement Points

- Per 802.3, timestamps are measured at the generic Reconciliation Layer
- 1588 / 802.1AS need timestamps representing the MDI
- Between the two is the PHY (plus MII)
- 802.3-2018 uses the estimated PHY delay (provided as a min and max value) to compensate for the PHY delay in the timestamps
- Timestamps are either measured at the first bit of frame data or first bit of SFD (802.3-2018 was not clear)

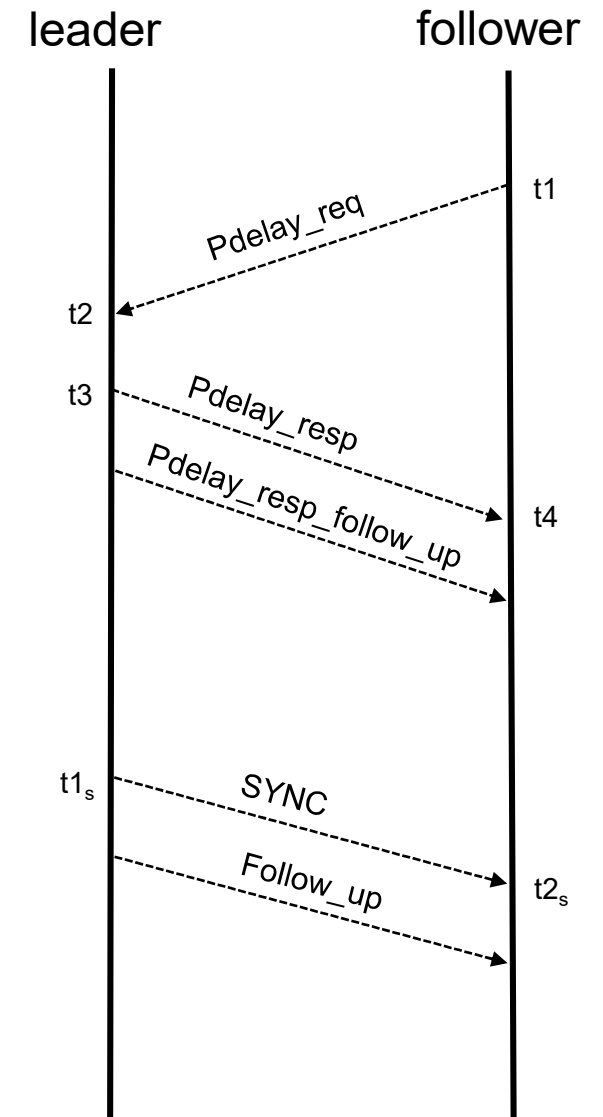


PHY Latency Variation

- PHY latency relates to the delay from MDI to MII in the Rx direction and from MII to MDI in the Tx direction
- PHY latencies vary due to multiple factors including
 - Different clock rates at the MII and MDI interfaces
 - Buffers of varying length
 - Clock domain crossings
 - Insertion / removal of idles
 - For PHYs including FEC, the position of the start of frame vs. the FEC block start
 - For multi-lane PHYs, buffer delays to align the lanes
- In this presentation PHY Latency Variation refers to the maximum absolute value of the difference between the expected PHY latency and the actual PHY latency
 - MaxPhyLVRx refers to the difference in the Rx direction
 - MaxPhyLVTx refers to the difference in the Tx direction
 - MaxPhyLV is the roundtrip delay difference (Rx and Tx)

PHY latency variation effects on 802.1AS

- PHY latency variation can affect
 - Propagation delay measurement
 - Maximum pdelay error due to latency variation is MaxPhyLV
 - Sync time accuracy
 - Maximum error in calculating time at Sync Rx is equal to the MaxPhyLVTx on the leader PHY plus the MaxPhyLVRx on the follower
 - Worst time error could be 2x MaxPhyLV due to a combination of pdelay & sync error
 - GmRateRatio calculations
 - computeGmRateRatio allows any scheme to be used
 - But spec requires +/-0.1ppm maximum error in the rate ratio calculation itself, but says nothing about timestamp accuracy
 - Worst case calculation (using previous 2 sync values) could lead to additional 2x MaxPhyLV error
- Asymmetric PHY latency variation can cause further inaccuracies



PHY latency variation effects on 802.1Qbv

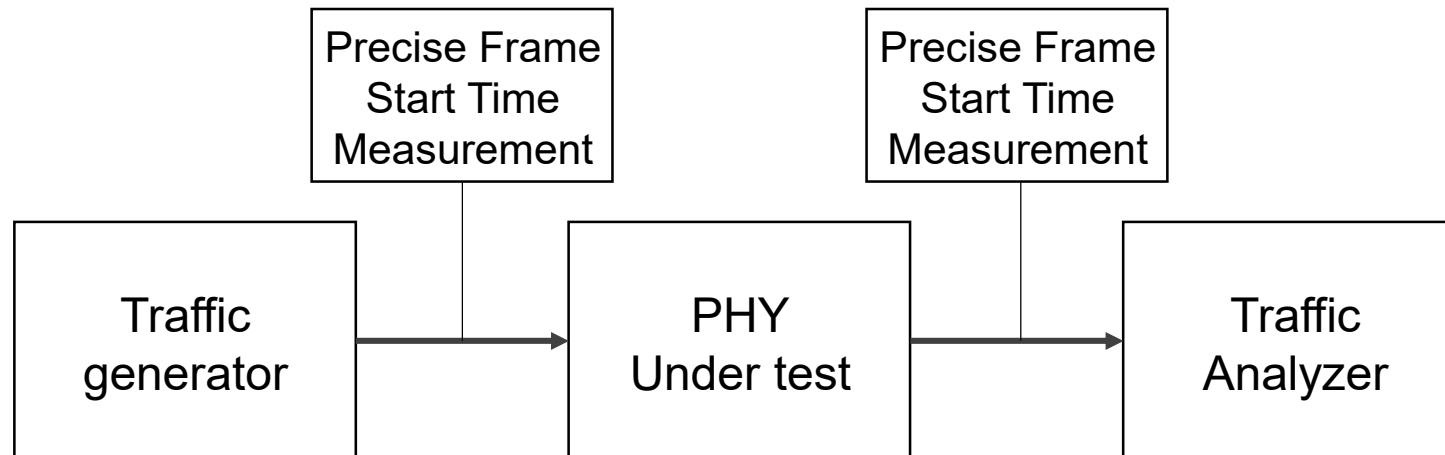
- Longer than expected PHY latency can cause frame transmission to end as much as MaxPhyLV after the gate close time
- Shorter than expected PHY latency can cause frame transmission to start as much as MaxPhyLV after the gate open time
- These can cause
 - Delay of priority frames by up to MaxPhyLV
 - Not enough bandwidth being allocated to a queue
 - Buffer overflow due to gate being open longer than expected

Proposed 802.3cx Ethernet timestamping improvements

- Provides a mechanism in the 802.3 spec for a PHY to report the dynamic PHY delay changes to the MAC
 - If implemented this could be provided per frame and compensate for delays in the PHY
 - This allows for a specification-compliant implementation that actually measures timestamps in the PHY instead of the generic Reconciliation Sublayer (gRS)
- Provides configurable selection of either the first bit of frame data or first bit of SFD as the delay measurement point in the frame
 - Previous version of 802.3 left this unclear
 - Allows an implementation to support either or both choices, and enables selecting one
 - Spec recommendation is to use first bit of data
- Provides clarity on timestamps should work with PHYs with multiple lanes, FEC, and insertion/removal of IDLE to avoid adding time uncertainty due to these functions
- Adds support for sub-ns timestamping resolution

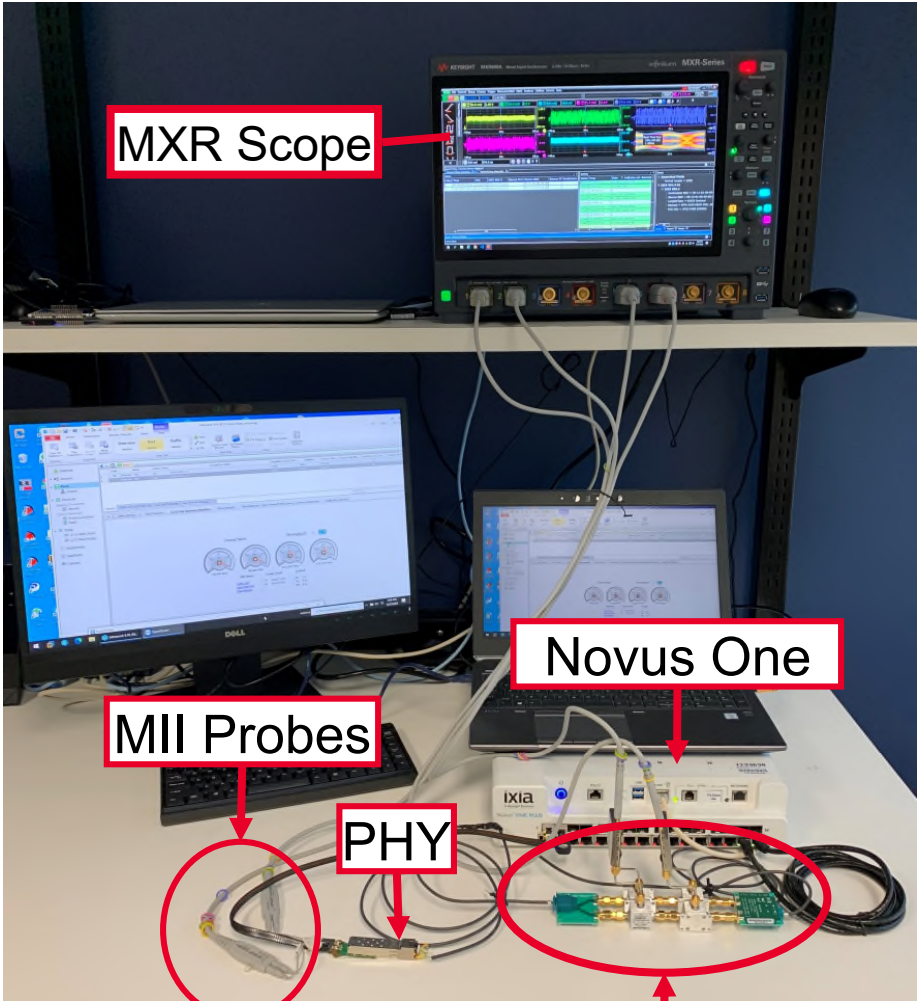
PHY Latency Characterization

- Connect test equipment to the PHY such that the time the frame starts can be ascertained at both the MII and MDI interfaces
 - Both Tx and Rx direction measurements are needed
- Configure the PHY in the same way it would be configured in the device
- Send traffic through the PHY and measure the latency of hundreds of thousands of frames
 - Must test a mix of all possible frame sizes
 - Must test with different inter-frame gaps, including minimum
 - Instrumentation must support measuring delay of consecutive frames
 - Instrumentation must validate that received frame matches transmit frame (any corrupted frames need to be excluded; guarantees that we are comparing the same frame at input and output)



Latency Measurement setup – 100BASE-T1

PHY Latency Measurement Setup



Zoom on MDI Probe including directional couplers and probes



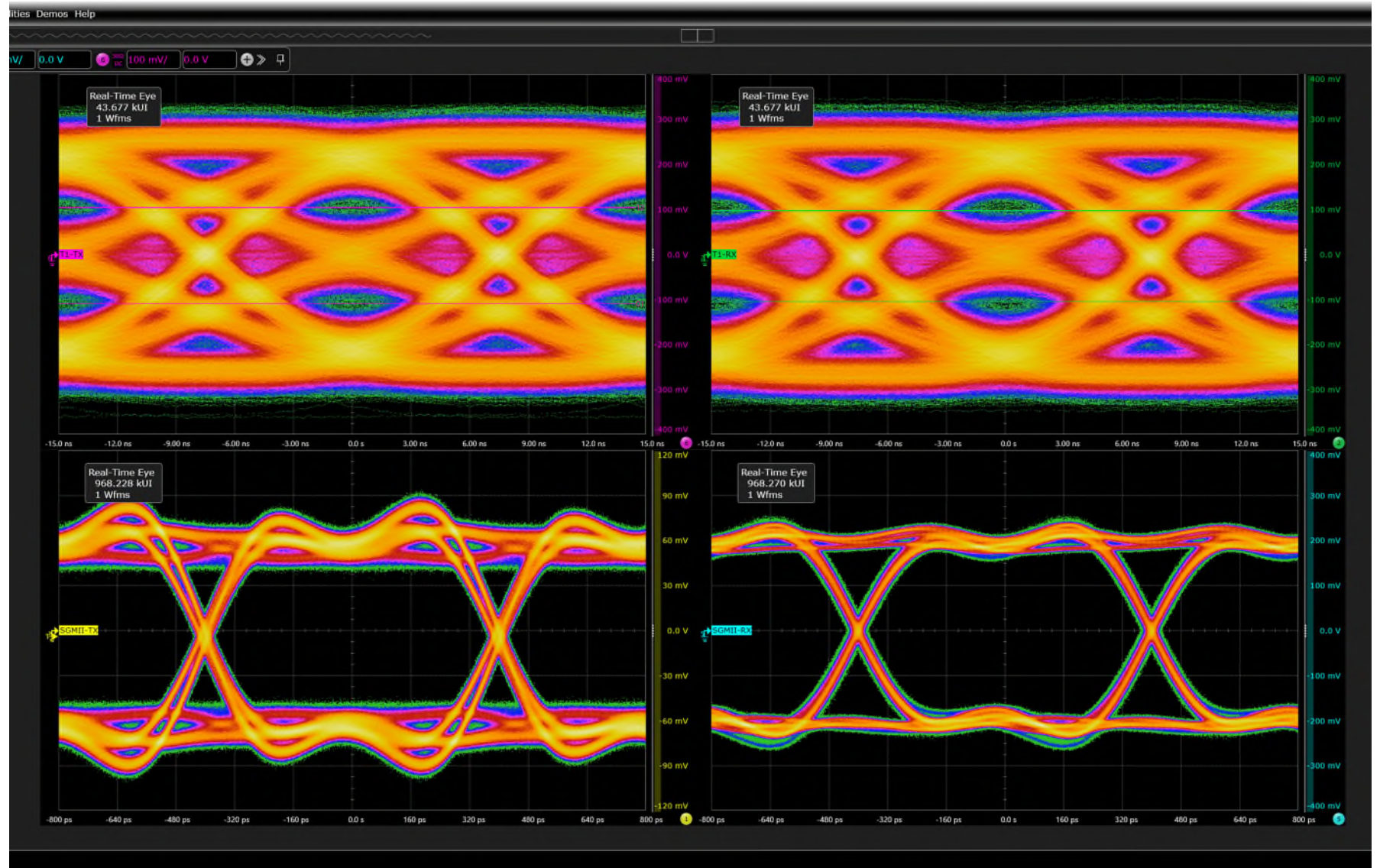
Signal eye diagrams

TX

RX

MDI:
100BASE-T1
PAM3

MII:
SGMII

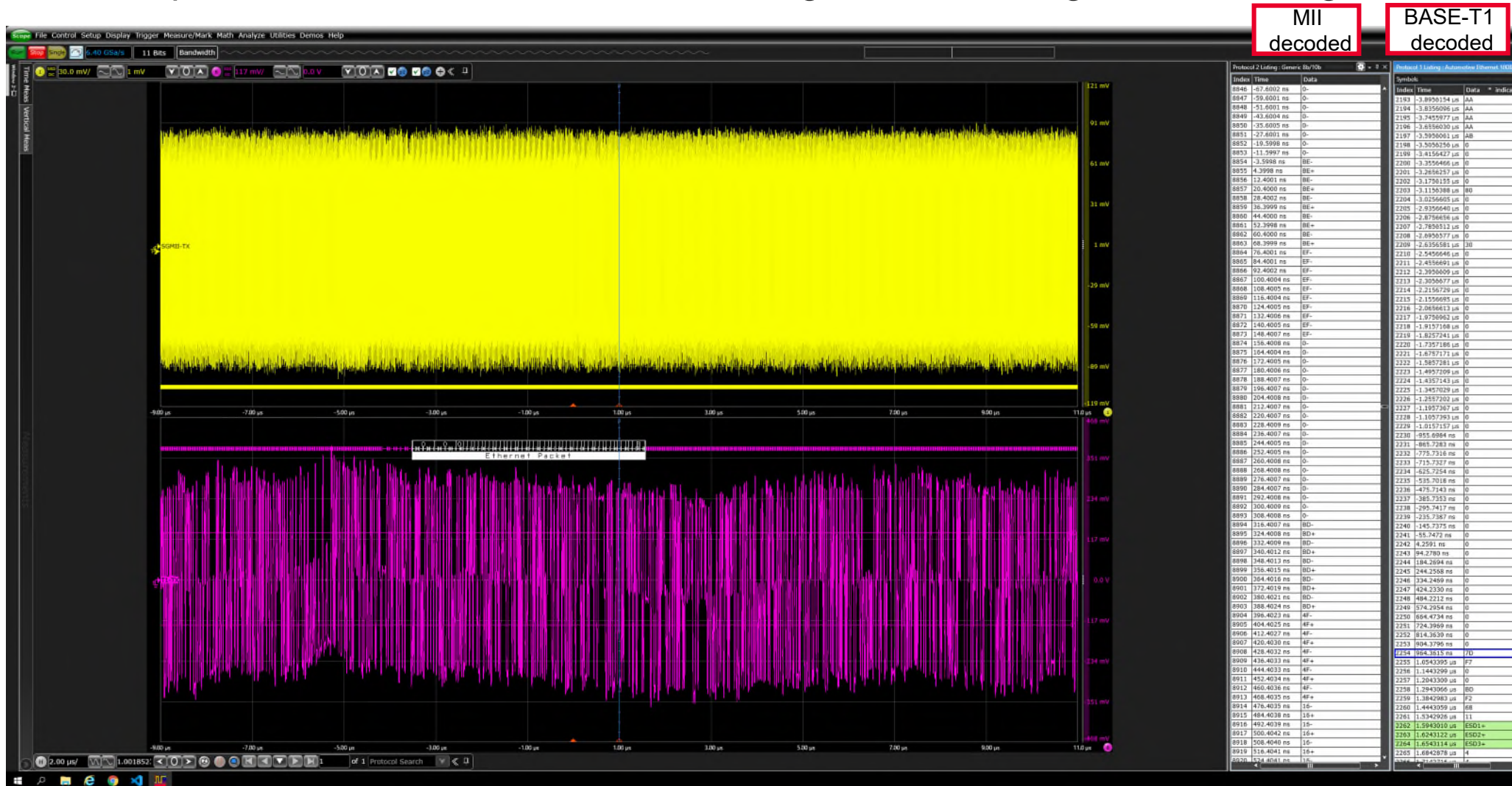


Protocol decode

- In order to detect SFD, protocol has to be decoded, including PAM decoding, descrambling, and alignment)

MII:
SGMII

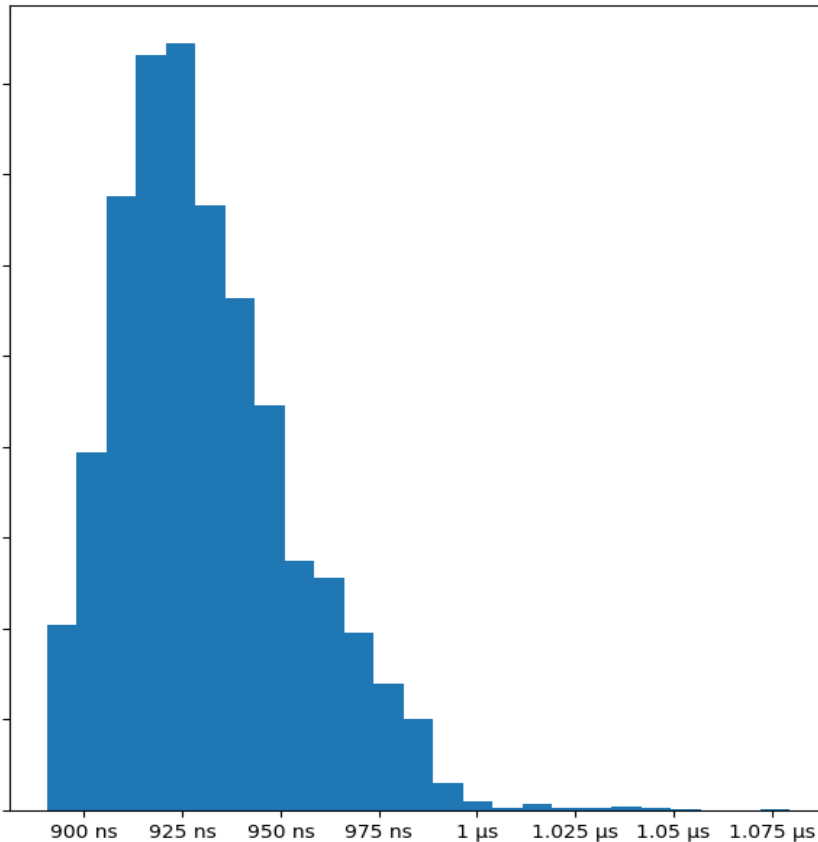
MDI:
100BASE-T1
PAM3



Measurement Results – Sample PHY 1 – 100BASE-T1

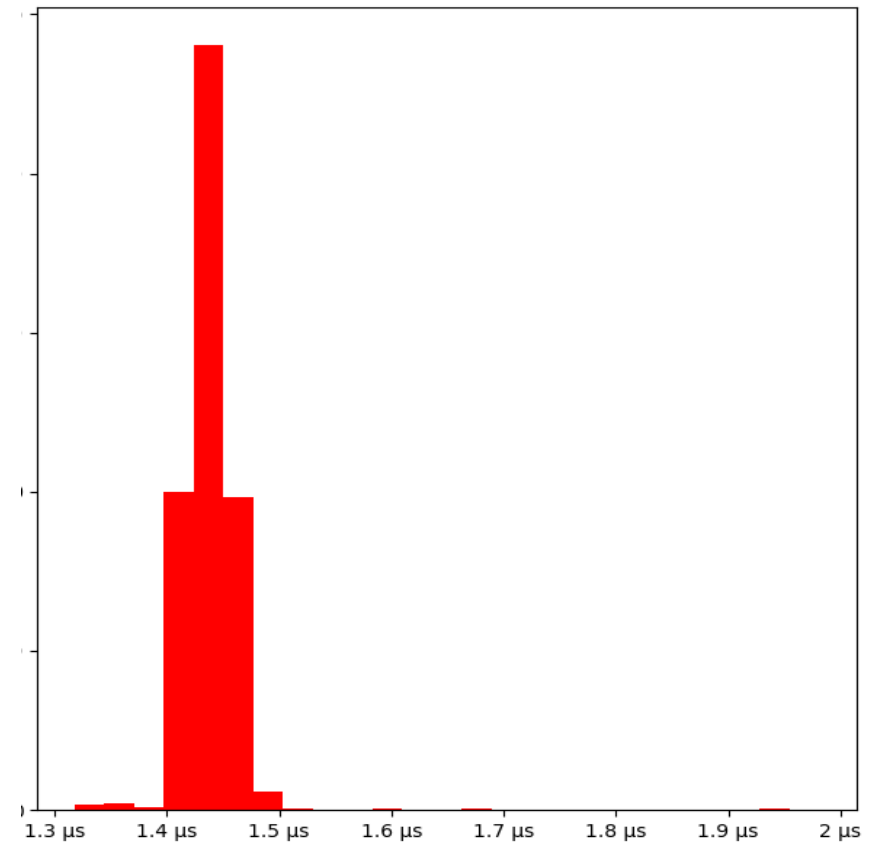
Tx (SGMII to 100BASE-T1):

Min: 890.5 ns Range: 189.0 ns
Ave: 931.3 ns Std Dev: 23 ns
Max: 1079.5 ns



Rx (100BASE-T1 to SGMII):

Min: 1318.0 ns Range: 663.2 ns
Ave: 1439.3 ns Std Dev: 32 ns
Max: 1981.2 ns

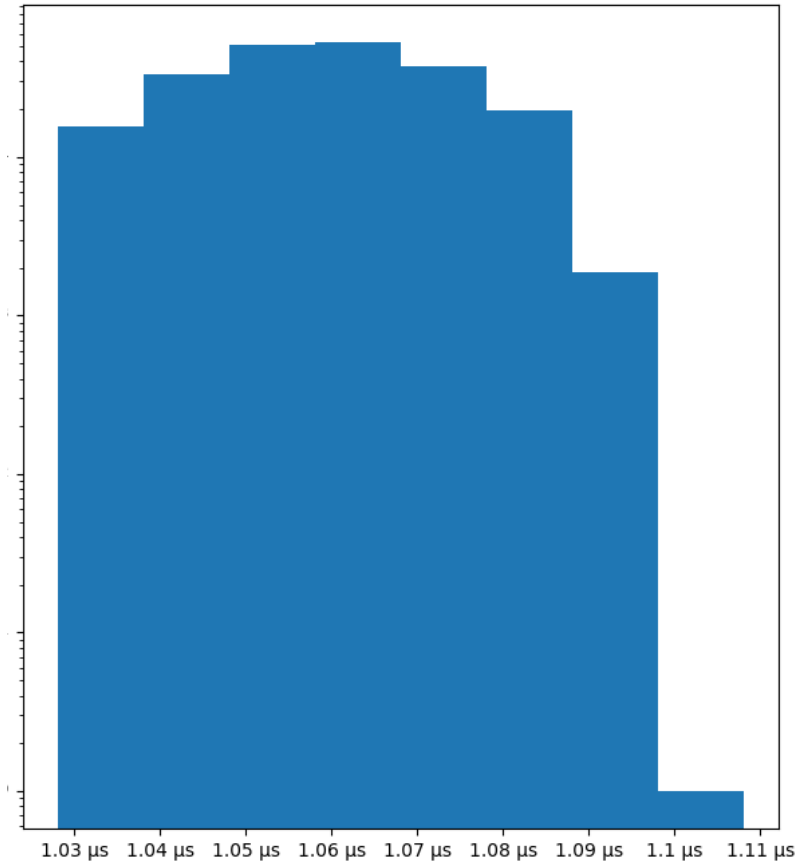


64 byte packets at 50% line rate (additional tests showed that packet size/mix and rate does not significantly affect results on this PHY)

Measurement Results – Sample PHY 2 – 100BASE-T1

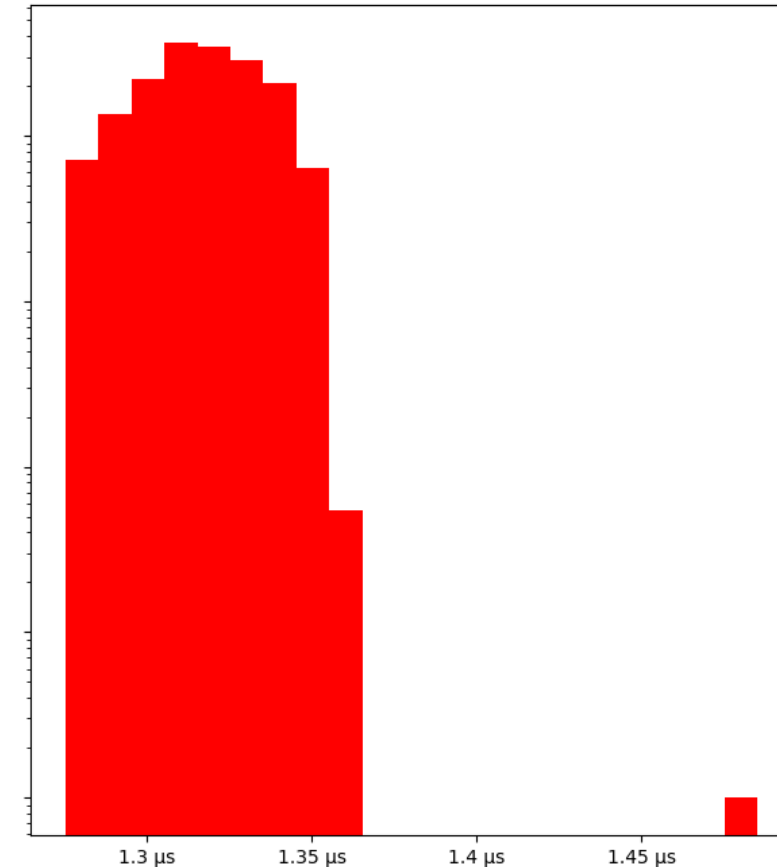
Tx (SGMII to 100BASE-T1):

Min: 1028.1 ns Range: 70.0 ns
Ave: 1059.2 ns Std Dev: 14.5 ns
Max: 1098.1 ns



Rx (100BASE-T1 to SGMII):

Min: 1275.2 ns Range: 202.6 ns
Ave: 1316.7 ns Std Dev: 17.3 ns
Max: 1477.8 ns



64 byte packets at 50% line rate (additional tests showed that packet size/mix and rate does not significantly affect results on this PHY)

PHY performance

- PHY selection is a critical part of the design of TSN equipment
- PHY performance, including PHY latencies and latency variation needs to be known
 - Latency & latency variation is dependent on PHY configuration
 - Most PHY datasheets do not list PHY latency and variation
 - Even ones that do are often wrong
- Selection of MII interface can have a big impact on PHY latency and latency variation
 - For example, SGMII will often have more latency variation than MII/GMII/RMII/RGMII due to additional clock crossings and buffers
- Enabling features in the PHY such as MacSEC or even (g)PTP timestamping can change the PHY latency!!
- PHY latency & latency variation can change when PHY silicon revision or firmware changes
- It is important to make sure PHY is properly characterized to avoid surprises later

Potential mitigations to PHY limitations

- Choose the MII interface mode with the lowest latency variation
- Do not use PHY features that increase latency variation
- Make sure the PHY latency compensation in the MAC / NIC can be adjusted to accommodate different PHY / PHY revision / PHY firmware
- Use PHY to timestamp (g)PTP frames
 - May help with 802.1AS, but requires servo to synchronize time between PHY & other system components
 - May be limited as to rate of 802.1AS frames, specific encapsulations, etc.
 - Does not solve 802.1Qbv latency variation issues
- Use alternative methods of measuring Frame Tx or Rx times
 - Some PHYs can provide a pulse per each frame Tx / Rx start
 - Sometimes these can be fed back to the MAC/NIC to enable more accurate timestamping
 - As with PHY timestamping, helps with 802.1AS, but not with 802.1Qbv latency variation

Summary and Recommendations

- PHY latency and latency variation can be very different on different PHYs
- The latency & variation affect 802.1AS, 802.1Qbv, as well as any other protocol relying on accurate delay measurement / compensation
- PHY selection & characterization is a critical part of building any TSN device
- Module / device manufacturers should
 - Require PHY vendors to document and guarantee their PHY latency performance
 - Choose a PHY configuration and MII interface that meets their PHY latency performance requirements
 - Characterize the PHY to make sure it meets stated requirements
- PHY manufacturers should
 - Strive to minimize (or provide means to minimize) PHY latency variation
 - Document PHY delays & range as required by IEEE 802.3-2018
 - Implement p802.3cx when approved

Questions?



Alon Regev

Alon.regev@keysight.com

dave.cavalcanti@intel.com



Marty Gubow

martin_gubow@keysight.com

alon.regev@keysight.com

Thank you