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# ***USE OF TSN FOR WHEEL SENSOR DATA IN A ZONAL ARCHITECTURE***

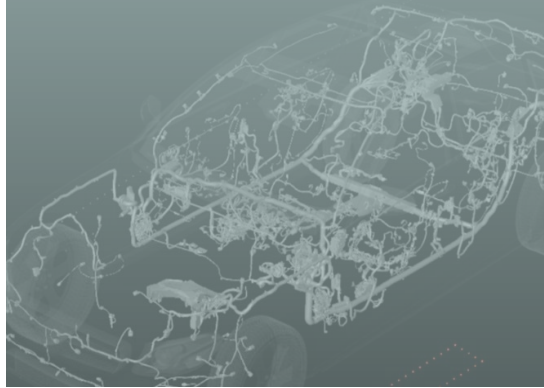


# Advanced Architecture Challenges

EXISTING ARCHITECTURES ARE NOT SUSTAINABLE IN A FUTURE OF CONNECTED AND AUTONOMOUS CARS

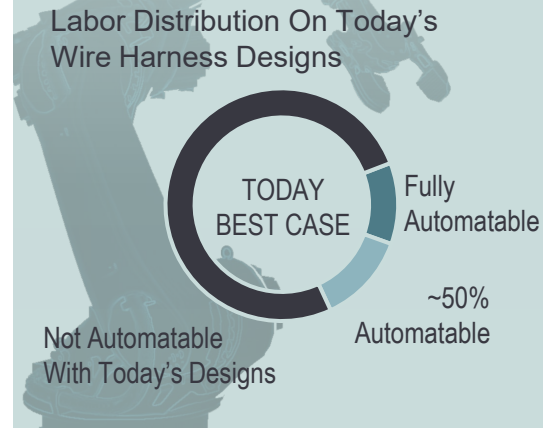
## COMPLEXITY

100+ controllers with many different variants running 200M+ lines of code that supports thousands of inter-dependent functions spread across multiple ECUs



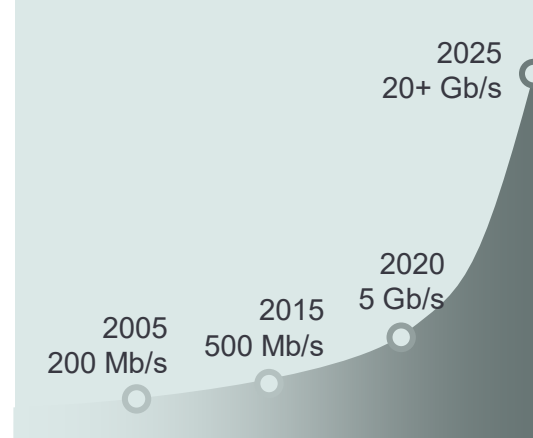
## LABOR COST

Direct manufacturing labor rates expected to increase 25% to 50%+ depending on location over next 5 years, but current designs do not support automation required to offset



## QUALITY OF SERVICE

Connectivity solutions demanding high bandwidth, fault tolerant vehicle networks operating on miniaturized hardware with increased wire density



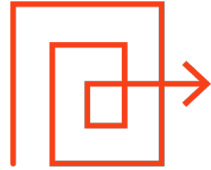
## AUTOMATED DRIVING

Driver out of the loop functionality (L3 and above) will require fail-safe operational performance, but redundancy is not an option despite due to cost or physical space

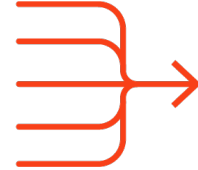


# Zonal Architecture Objectives and Design Philosophy

## Architecture Objectives



**SIMPLIFY**  
More Function  
in Fewer Boxes

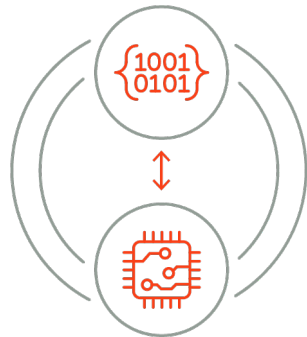


**UNITE**  
Diverse Applications  
Across the Full Vehicle  
Lifecycle

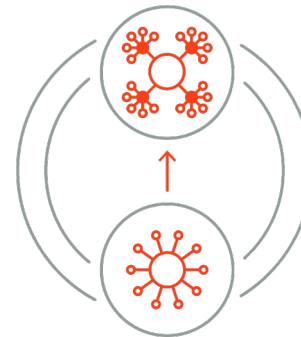


**EMPOWER**  
OEMs to Fully Control  
the User Experience of  
Their Vehicles

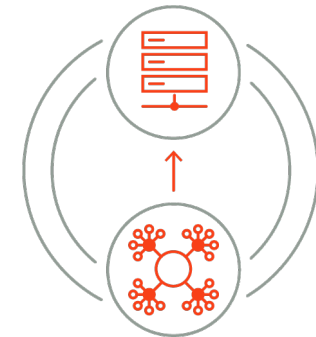
## Design Philosophy



**ABSTRACT**  
Software From Hardware



**SEPARATE**  
Input / Output From Compute

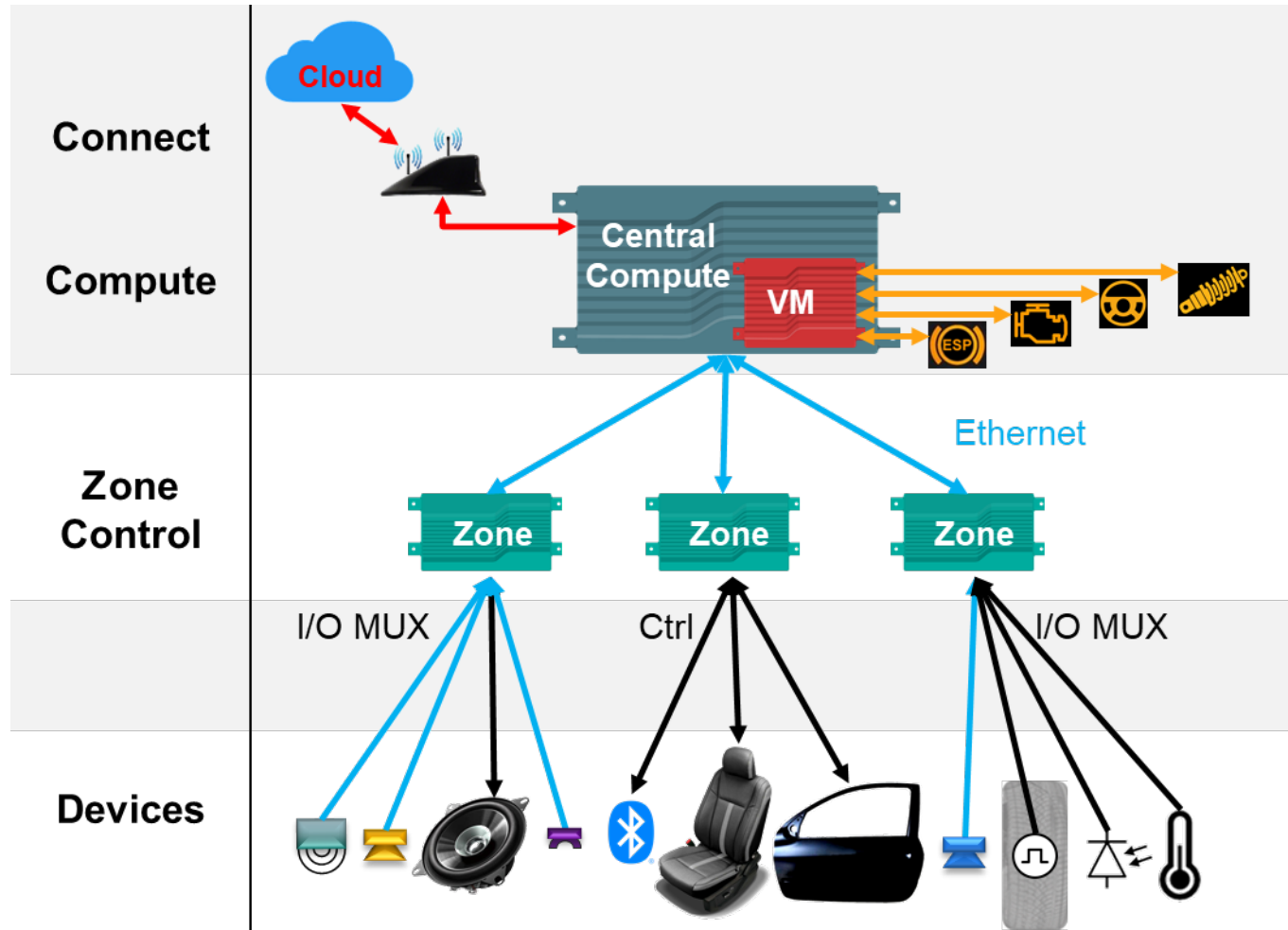


**ENABLE**  
“Serverization” of Compute

# Multi-Layer Zonal Based Architecture

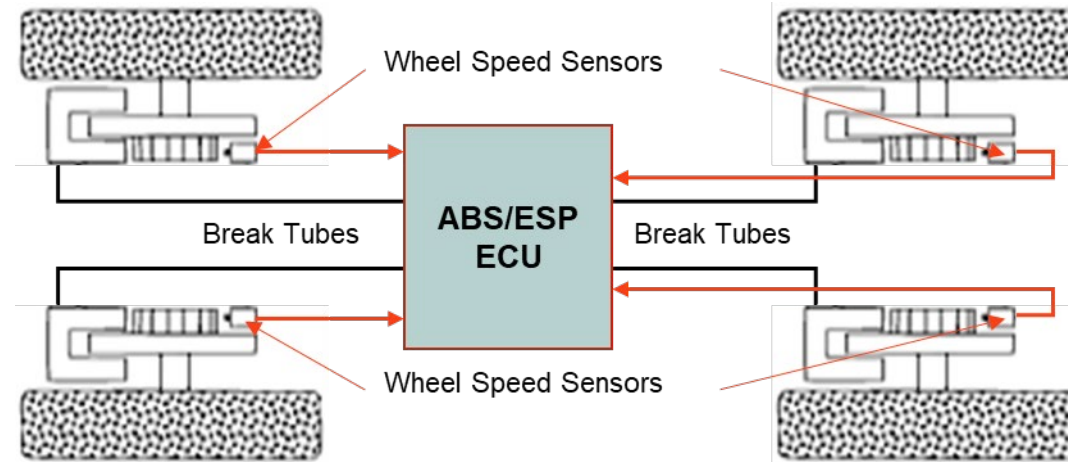
## Zonal Architecture

## Functions



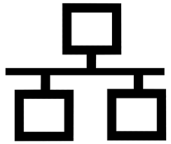
- Connectivity**  
Wireless connectivity, Edge and Cloud Services
- Central Compute**  
Body & Power, Network, Gateway, ADAS/AD, Infotainment
- Vehicle Motion**  
Braking, Steering, Dampers and Engine applications
- Zone Controller**  
I/O Abstraction, Data aggregation, Power Supply, Body functions
- SENSORS / ACTUATORS**  
Radar, Lidar, Camera and Ultrasonic sensors, direct controlled sensors, actuators or ECUs (e.g. door modules, seat controller)

# Wheel Speed Sensors in Current ABS/ESP Systems

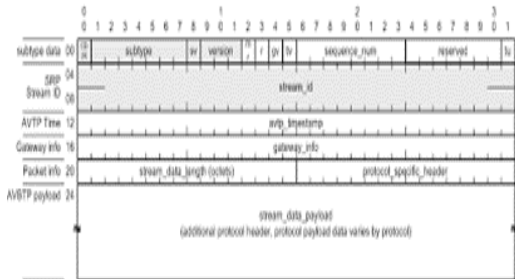


- ABS/ESP Systems Include Several Sensors
  - Wheel Speed, Steering Angle, Yaw Rate, 3D Acceleration
- Wheel Speed Sensors on Each Wheel:
  - Generating a fixed number of electrical pulses per rotation
  - Sensor data is time critical, maximal allowed delay is  $<1\text{ms}$
  - Currently ALL wheel speed sensors connect DIRECTLY to the ABS/ESP ECU

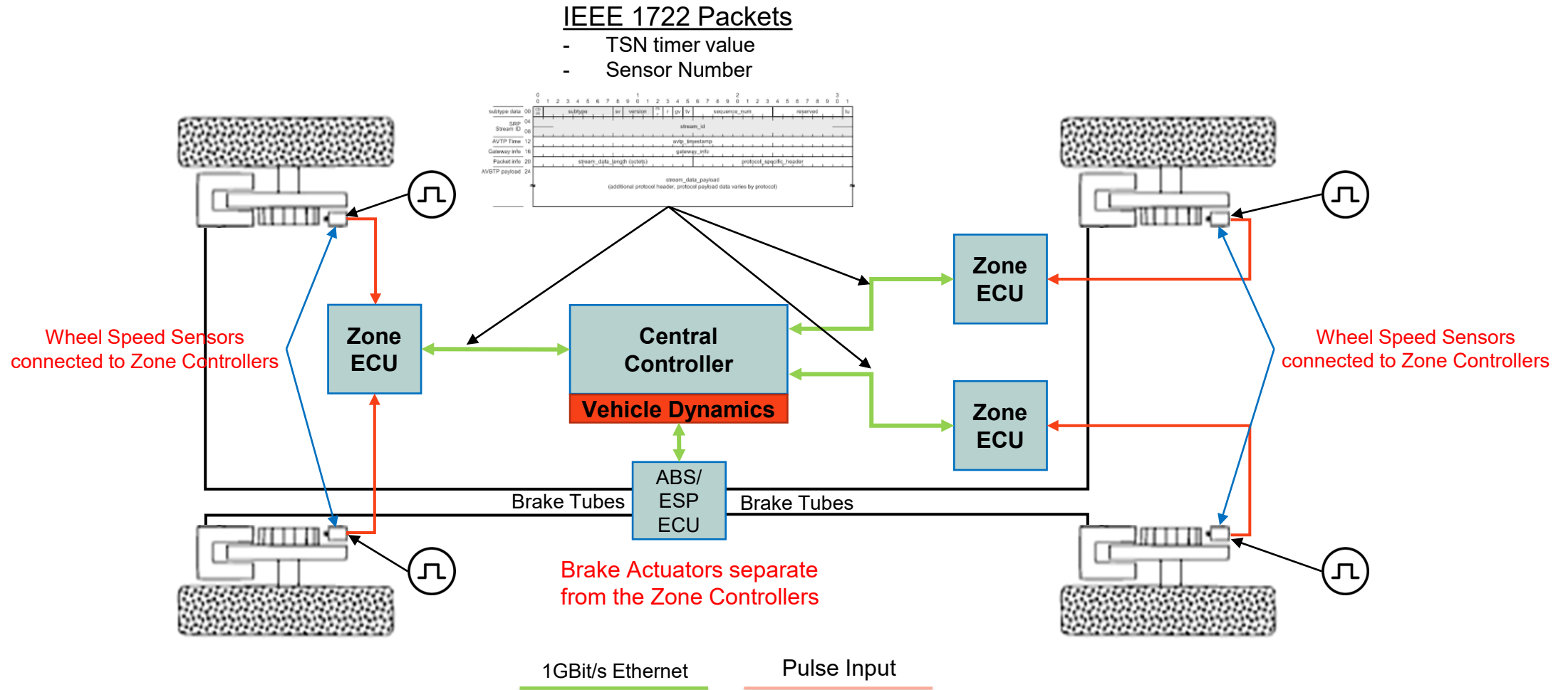
# Wheel Speed Sensing in a Zonal Architecture



- Wheel Speed Sensors Provide a Digital Signal:
  - Vehicle speed can be calculated from the distance of two consecutive pulses
  - Number of pulses per wheel turn is always constant
- Ethernet Based Network Connects Zonal Controllers to Central Compute Nodes
  - Ethernet TSN is mandatory (time critical applications and network redundancy)
- Concept: One Ethernet Data Packet on Each Rising Edge of Each Wheel Speed Sensor Pulse
  - IEEE 1722 data packets because of small protocol overhead
  - Wheel pulse packet payload:
    - 32bit Ethernet TSN timer value at the rising edge of the wheel pulse
    - 8bit Sensor number
    - 28 Pulses per wheel turn → 200Kph < 1KHz

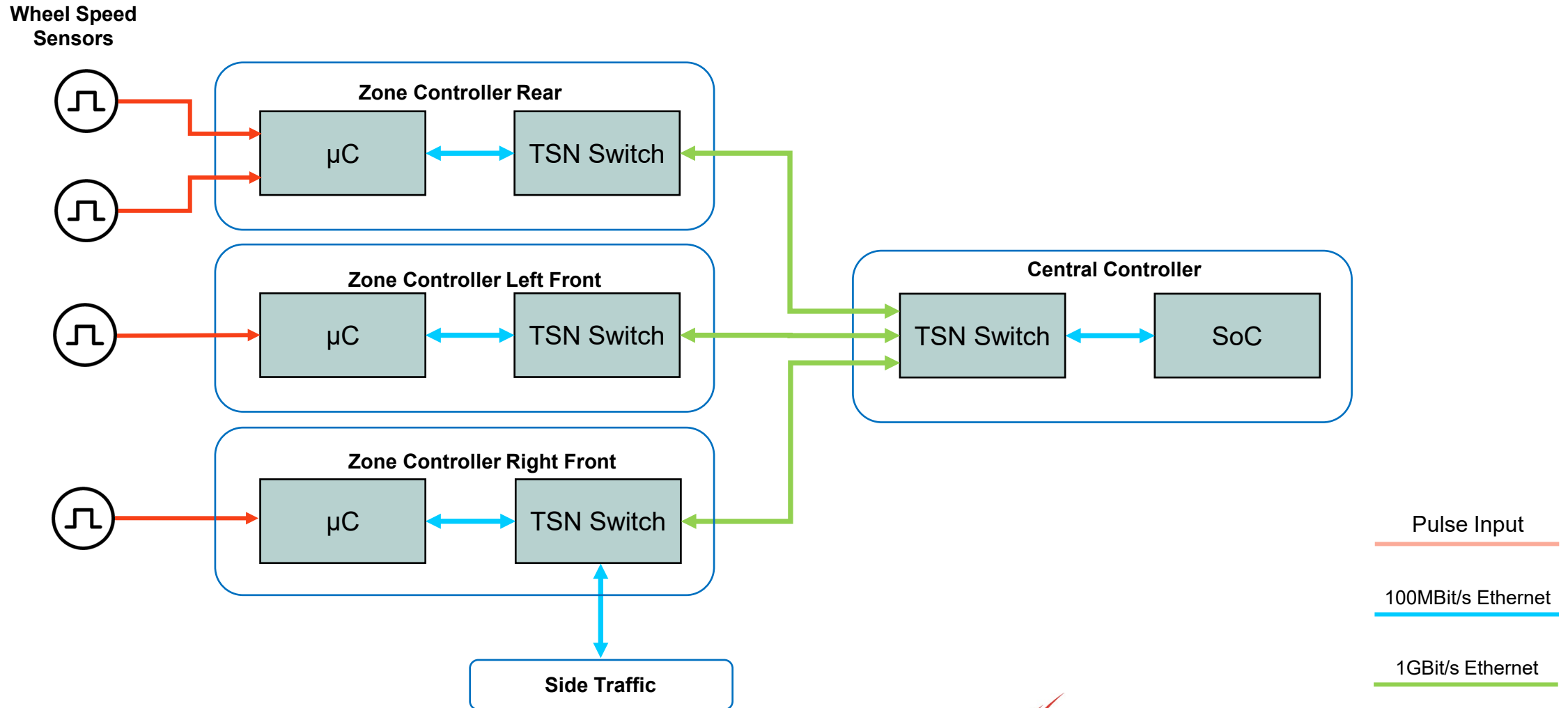


# Wheel Speed Sensing in a Zonal Architecture



# Wheel Speed Sensing System Concept

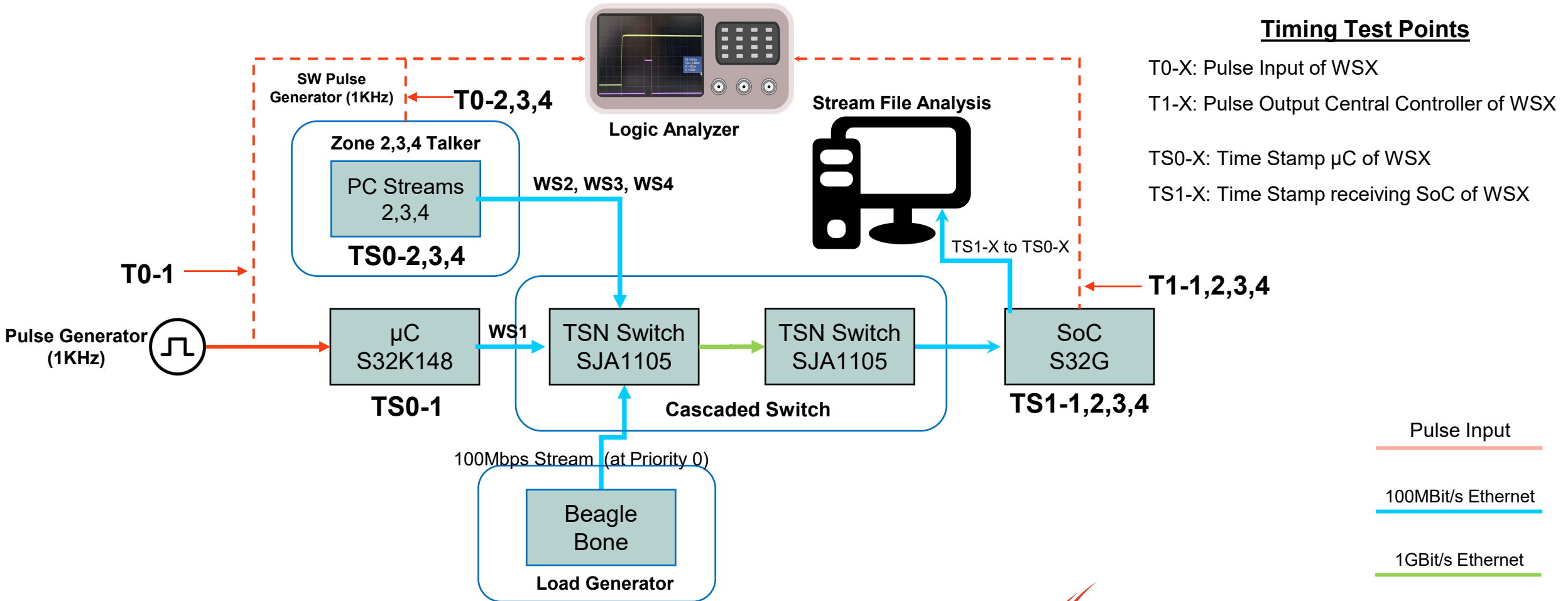
Four Asynchronous Talkers, Two Hops to Listener, Plus Side Traffic





# Test System Setup

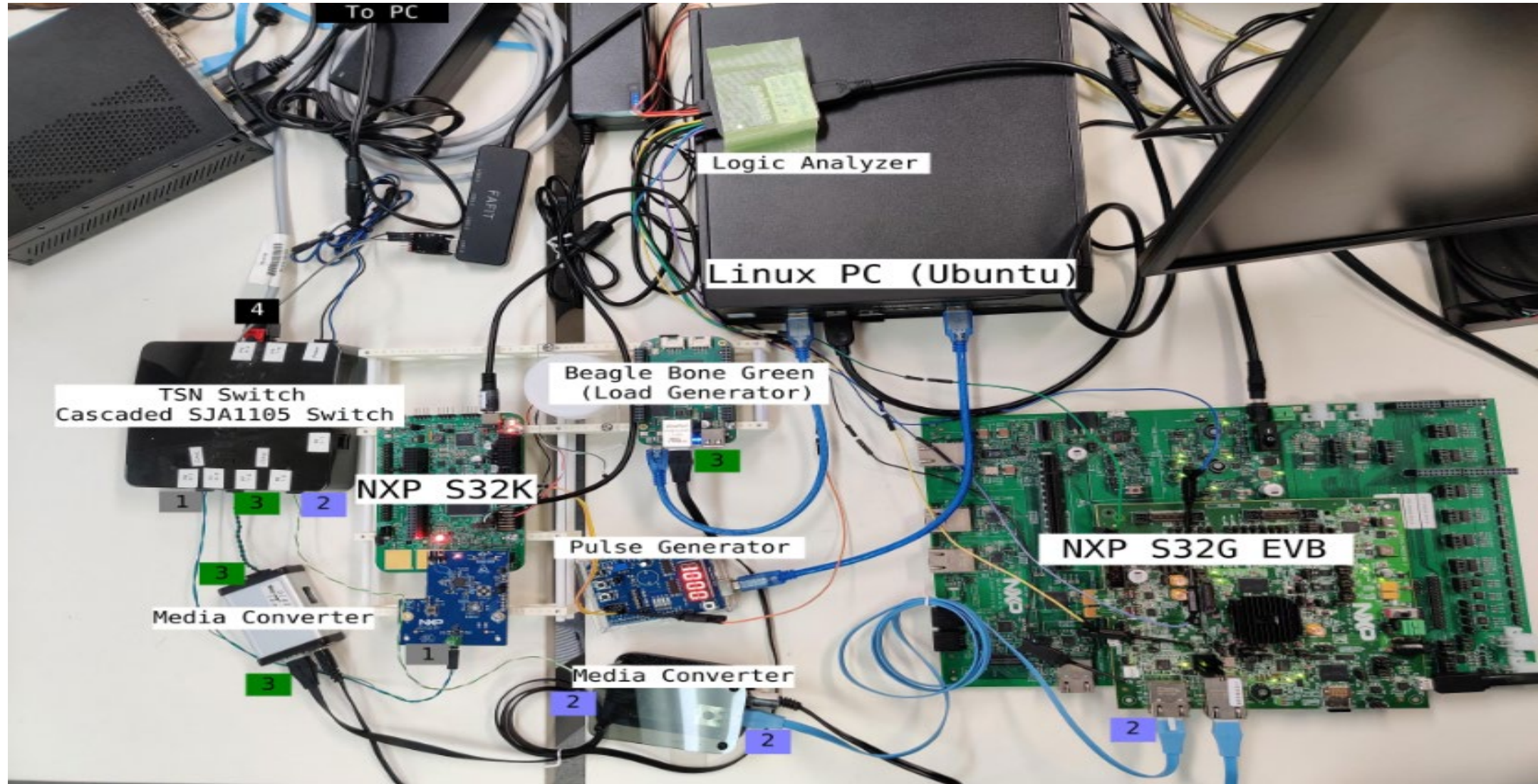
Four Asynchronous Talker Streams, Two Hops to Listener, Plus Side Traffic



# Test System Setup

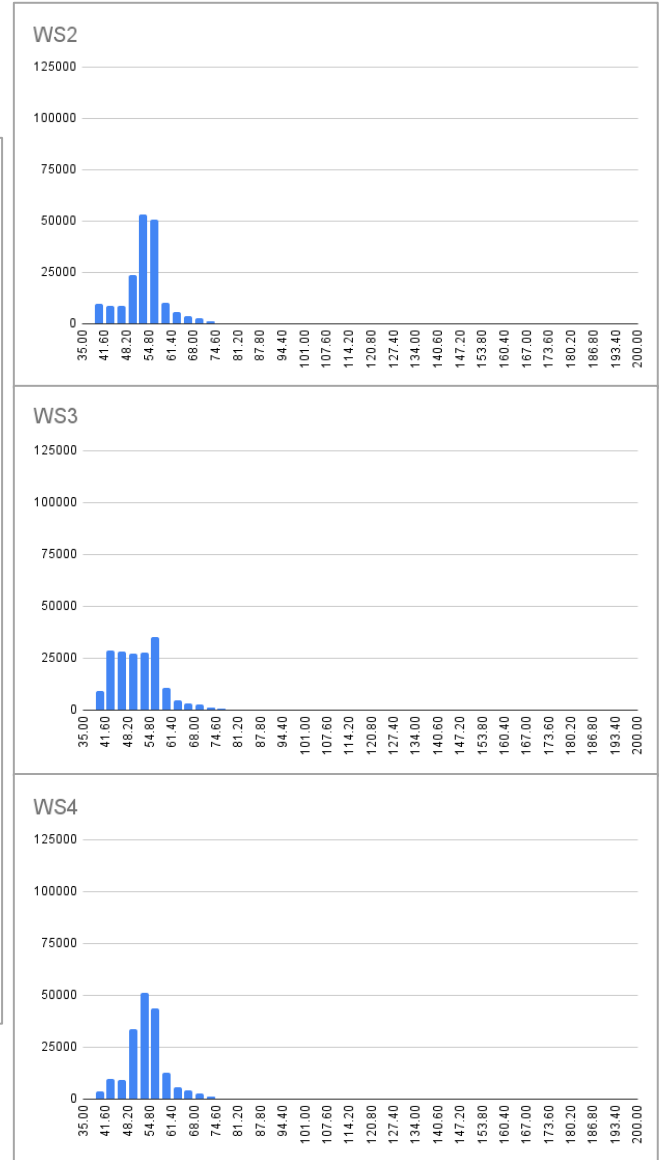
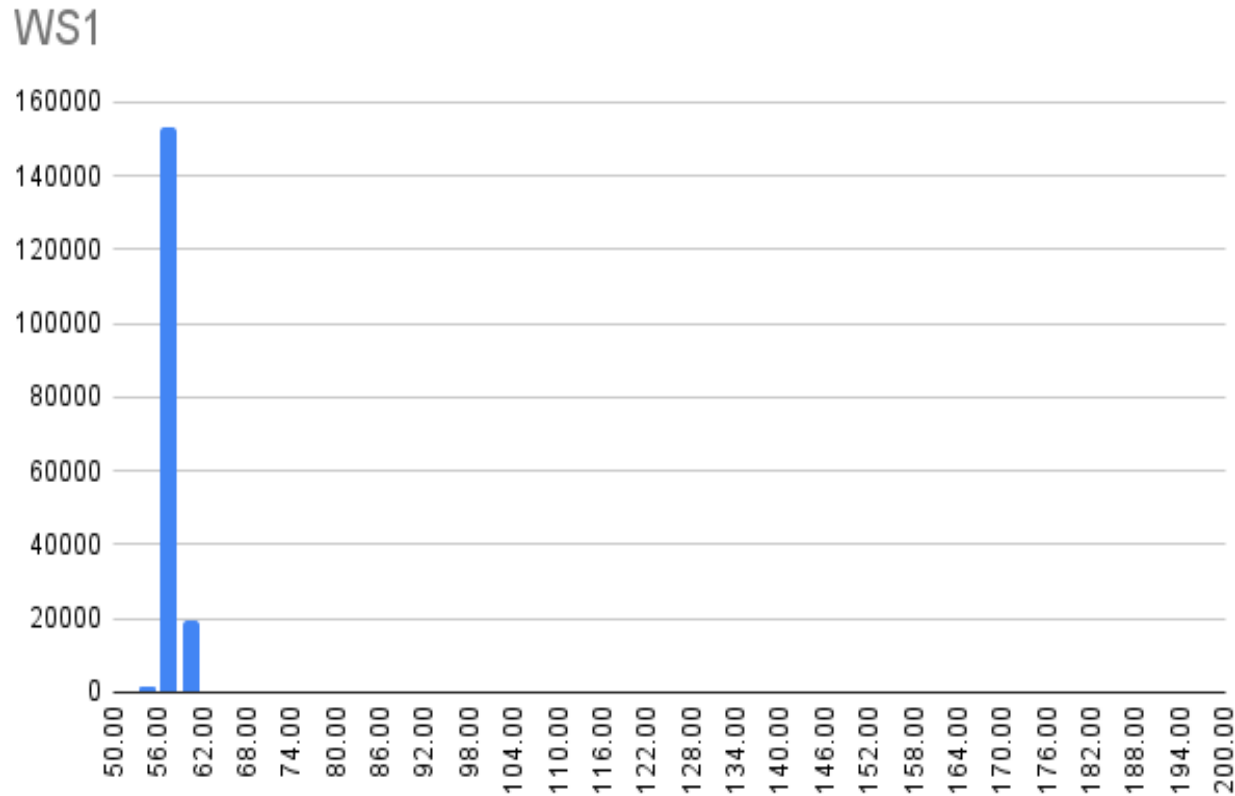
- Main Requirement Wheel Speed Sensing: <1ms Transport Delay to the Vehicle Motion Node
- Test Setup:
  - Zone Controller with S32K148 + Ethernet Switch SJA1105 (NXP):  $\mu$ C creates an IEEE1722 packet on Each Wheel Pulse
    - Priority = 2 (Highest Priority) Using 802.1Qav (FQTSS) Credit-Based Shaper
    - Payload = 32bit TSN Timer Value + 8bit Sensor Number
  - Zone Controller Emulator: PC creates 3 additional IEEE1722 streams (Priority = 2) to emulate multiple Zone Controllers
  - Load Generator, connected via 100MBit/s Ethernet port to the switch: Generating 100Mbps stream of lower priority (Priority = 0) traffic
  - Central controller with SoC S32G274 + Ethernet Switch SJA1105: S32G SoC receives 1722 packets and adds second Ethernet TSN time stamp, statistic analysis on a PC, comparing first and second TSN time stamp values in each 1722 packet
  - S32G board also generates a digital pulse for each packet it receives
  - Each wheel pulse and the generated pulse from the S32G visualized on the logic analyzer to compare with statistical analysis, to verify no significant delays from packet assembly and parsing

# Test Setup



# Test Results with No Side Traffic

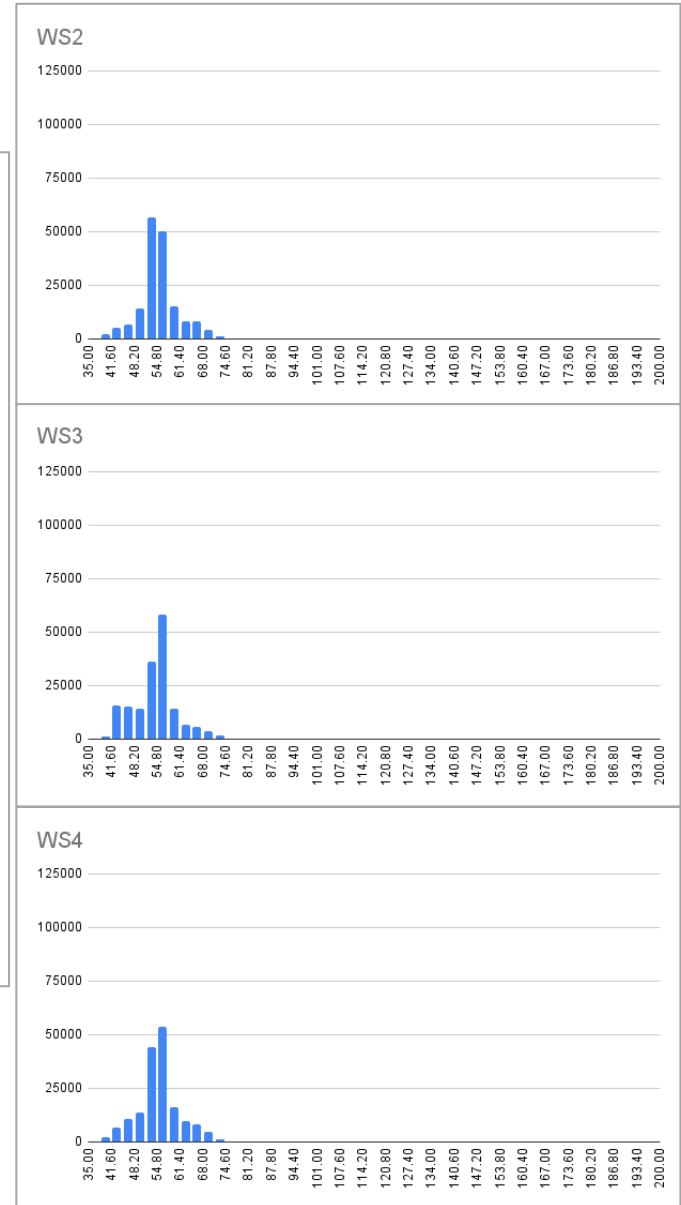
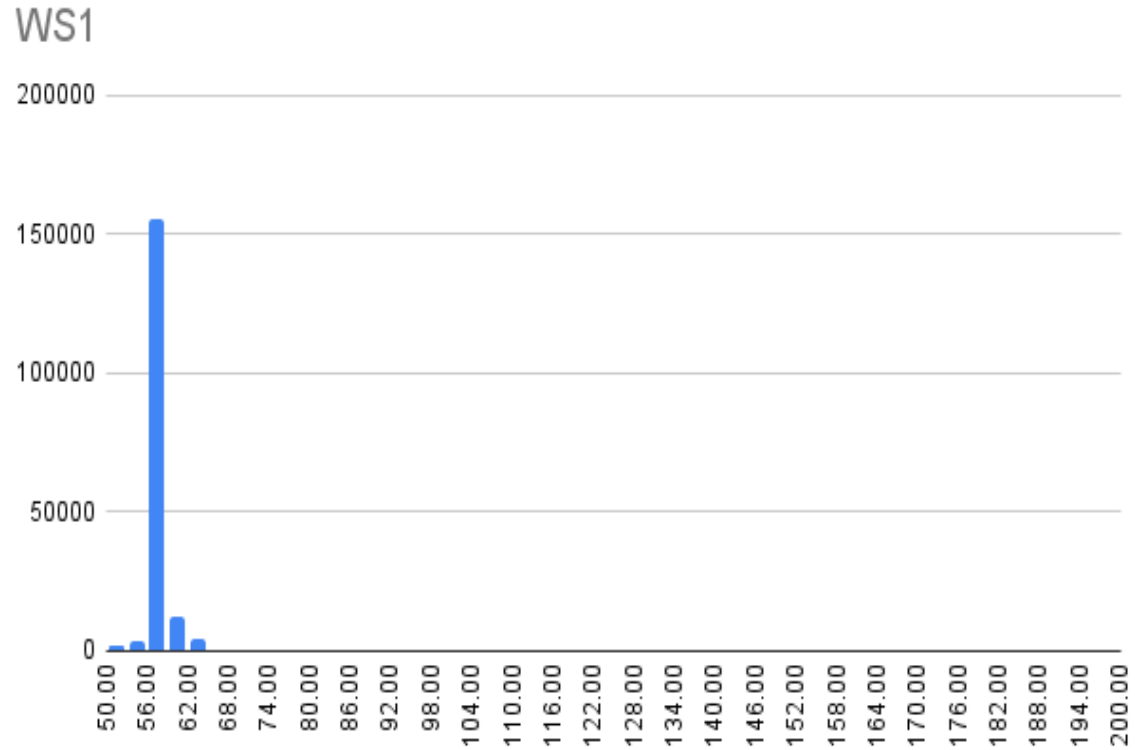
WS1 (S32K, Stream ID: 0x91e0f000fe010001)	
Test Settings	
Pulse Generator Frequency (Hz)	1000
Run time (minutes)	3
Total Data Count	173 424
Statistics (usec)	
Average	57.678
Median	57
Mode	57
Standard Deviation	0.9651
Maximum	61
Minimum	54
Quartiles	
Q1	57
Q3	58
IQR (Inter Quartile Range)	1
UOF (Upper Outer Fence)	61
LOF (Lower Outer Fence)	54



- WS1 Signal is the True Use Case / is the Superior Set-up
- WS2 – 4 are Proxy Signals Generated by Single PC – Show Wider Timing Variance
- In All Cases Total Latency < 85µSec

# Test Results with Side Traffic

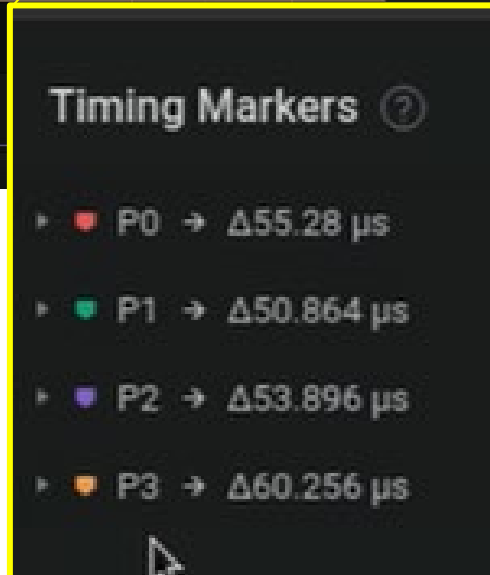
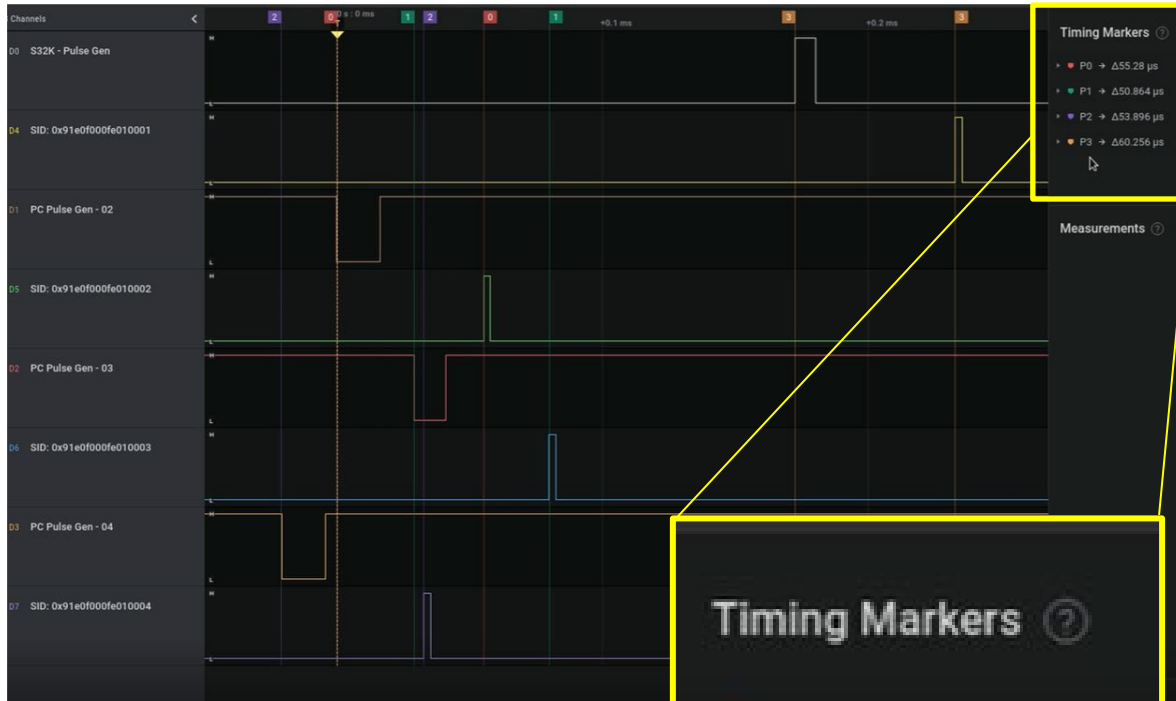
WS1 (S32K, Stream ID: 0x91e0f000fe010001)	
Test Settings	
Pulse Generator Frequency (Hz)	1000
Run time (minutes)	3
Total Data Count	176 631
Statistics (usec)	
Average	57.258
Median	57
Mode	57
Standard Deviation	1.450
Maximum	64
Minimum	50
Quartiles	
Q1	56
Q3	58
IQR (Inter Quartile Range)	2
UOF (Upper Outer Fence)	64
LOF (Lower Outer Fence)	50



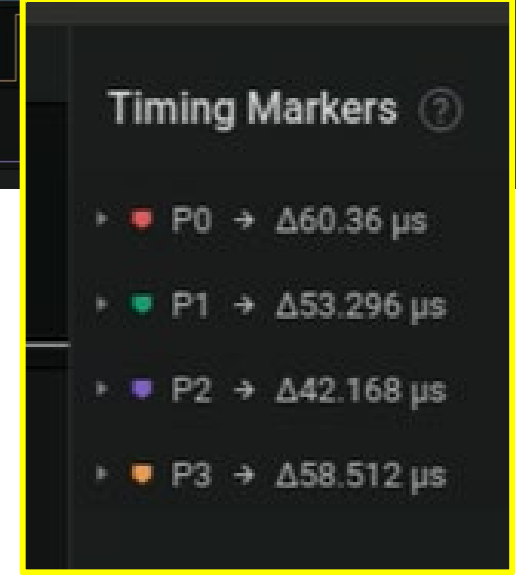
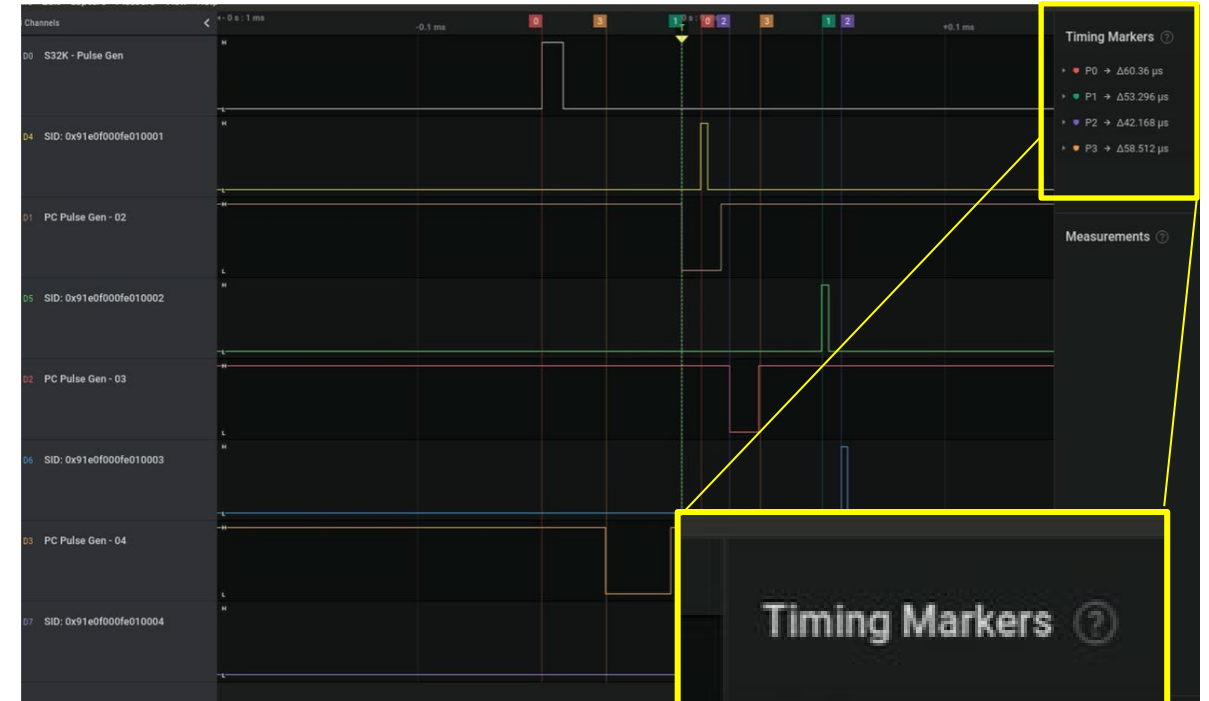
- Injecting Side Traffic has Little Impact on Latency of WS1
- WS2 – 4 Also Show Little Impact
- In All Cases Total Latency Remains < 85µSec

# Stream Files Verified by Scoping the Pulses

No Side Traffic

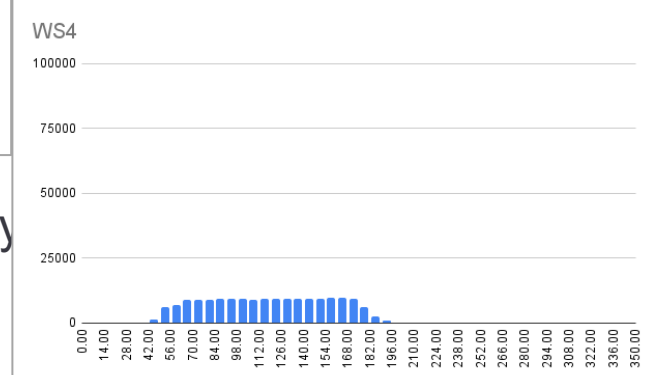
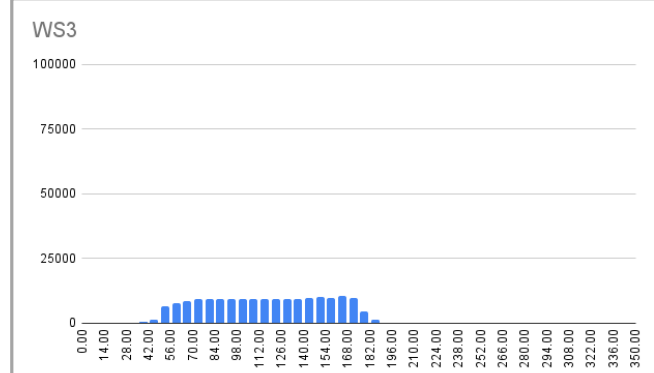
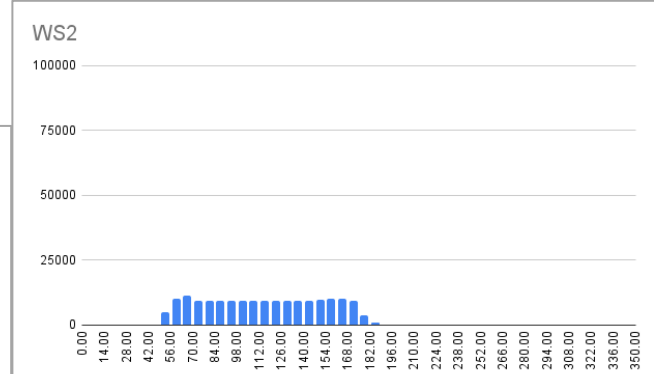
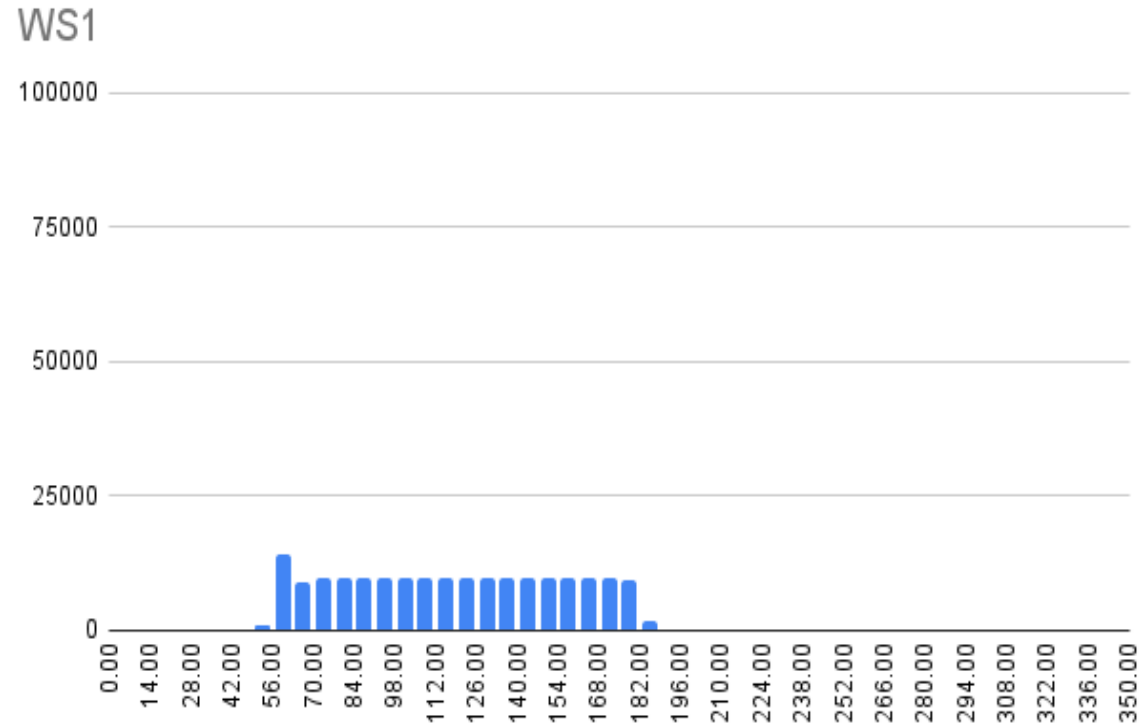


With Side Traffic



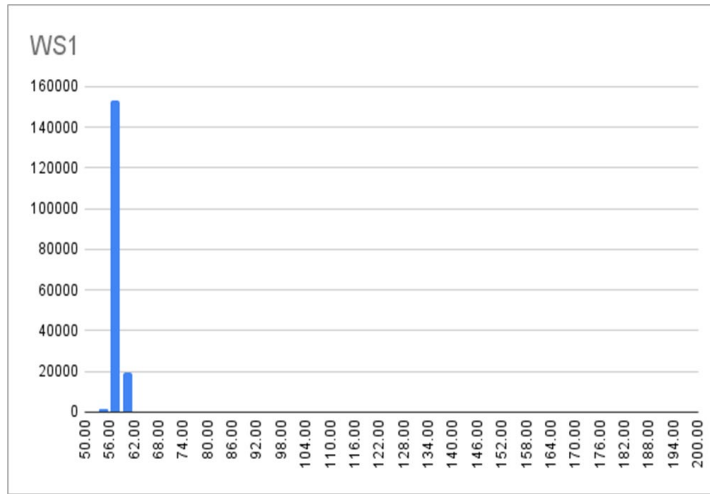
# Test Results with Side Traffic, No Traffic Shaping

WS1 (S32K, Stream ID: 0x91e0f000fe010001)	
Test Settings	
Pulse Generator Frequency (Hz)	1000
Run time (minutes)	3
Total Data Count	179 793
Statistics (usec)	
Average	117.550
Median	118
Mode	56
Standard Deviation	38.156
Maximum	345
Minimum	47
Quartiles	
Q1	85
Q3	150
IQR (Inter Quartile Range)	65
UOF (Upper Outer Fence)	345
LOF (Lower Outer Fence)	-110

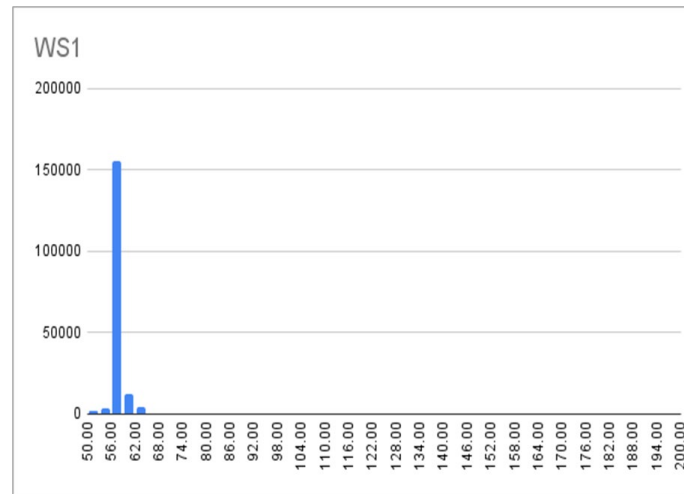


- Without Credit-Based Shaper/Priority 2 on WS Streams there is No Consistency
- Max Latency Jumps to 345  $\mu$ Sec
- Increases in Side Traffic Expand the Range of the Jitter

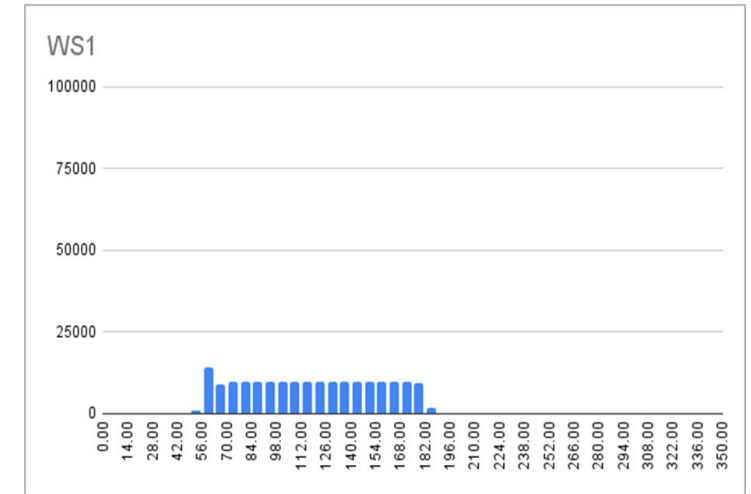
# Analysis of Test Results



Credit-Based Shaper P2 / No Side Traffic



Credit-Based Shaper P2 / Side Traffic



No Credit-Based Shaper P2

## With Credit-Based Shaper:

- Critical signals are not impacted by side-traffic
- P2 traffic will not be pushed from Queue so long as class is guaranteed sufficient bandwidth

## Without Credit-Based Shaper:

- If total network bandwidth exceeds traffic by wide margin, critical timing will be met
- BUT timing is not deterministic – as side-traffic expands the spread, can overrun the Queue



# Conclusions

- We Tested the Efficacy of Wheel Speed Sensors Signals Routed over TSN via a Zone Controller
- Conclusion:
  - Testing shows clear effectiveness of FQTSS Credit-Based Shaper regardless of side-traffic
  - 1Khz signal: 1Gbps TSN Network using Credit-Based Shaper (802.1Qav) is sufficient
    - Requirement on wheel speed sensing of <1ms latency is achieved under all test conditions
- Indications: (should be confirmed with further testing)
  - 1Khz signal: 100Mbps TSN Network with Credit-Based Shaper should be sufficient
  - Up to 4Khz signal: 1Gbps TSN Network with Credit-Based Shaper should be sufficient
  - TSN Network with Credit-Based Shaper should be sufficient provided that the bandwidth reserved for the priority class is greater than the traffic of the priority class, regardless of side traffic
- Up-Integration of Wheel Speed Signals into the Zone Controllers Offers Potential for Positive Effects to the System Architecture and Will Improve Harness Automation

The logo for Vexcelfore features a stylized red checkmark icon on the left, composed of two parallel lines that curve upwards and to the right. To the right of this icon, the word "vexcelfore" is written in a blue, lowercase, sans-serif font.

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• **A P T I V** •